SLM Clock & Delay Monitor IP

Measure delay between edges of a signal(s)

Highlights

- Accurate delay measurement between two edges
- No high-speed high accuracy reference clock required
- Low overhead for data processing
- Small form factor
- EDA integration for automated insertion and connection
- Capture state of silicon precisely at any stage of its lifecycle

Use Cases

- Clock insertion delay
- Clock duty cycle
- Memory access time
- Delay line characteristic
- Ring oscillator frequency

Overview

Synopsys SLM Clock & Delay Monitor (CDM) IP is a very small piece of IP, which can be inserted in silicon without much area overhead. It doesn't need any accurate high speed reference clock and provides accurate time delay measurement. It can be used for measuring clock duty cycle, memory access time, delay line characteristics, etc. It has IEEE 1500/1687 interface for connecting to test fabric. The SLM CDM IP is also available as an ISO 26262 ASIL-B ready product.

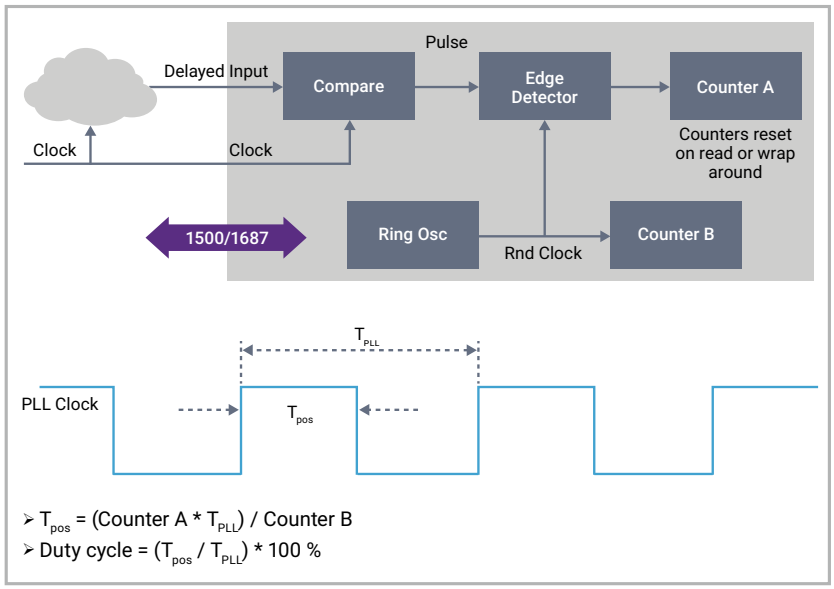

Figure 1: Synopsys SLM Clock & Delay Monitor IP

SLM Functional Monitors

Functional monitors are key to the success of Silicon Lifecycle Management (SLM). These monitors are embedded in the silicon and report out health of critical functions of the chip. Data from functional monitors can be collected at any stage of silicon lifecycle and analyzed to gather insights. Based on these insights actions can be taken to improve performance or mitigate an operational issue. Memory, CPU workload, interface, clock, delay, etc. are some critical functions on a SOC worth monitoring. Synopsys' functional monitors are enabled with EDA and software automation for ease of use.

Key Features

- No high-speed high accuracy reference clock required
- Small footprint
- Available as soft IP with flexibility to customize

Key Benefits

- Clock duty cycle quality check
- Memory access time tracking with BIST
- Digital delay line test characterization
- Optimize silicon performance for safety critical applications

Complete solution in SHS/SMS environment for Memory Read Time

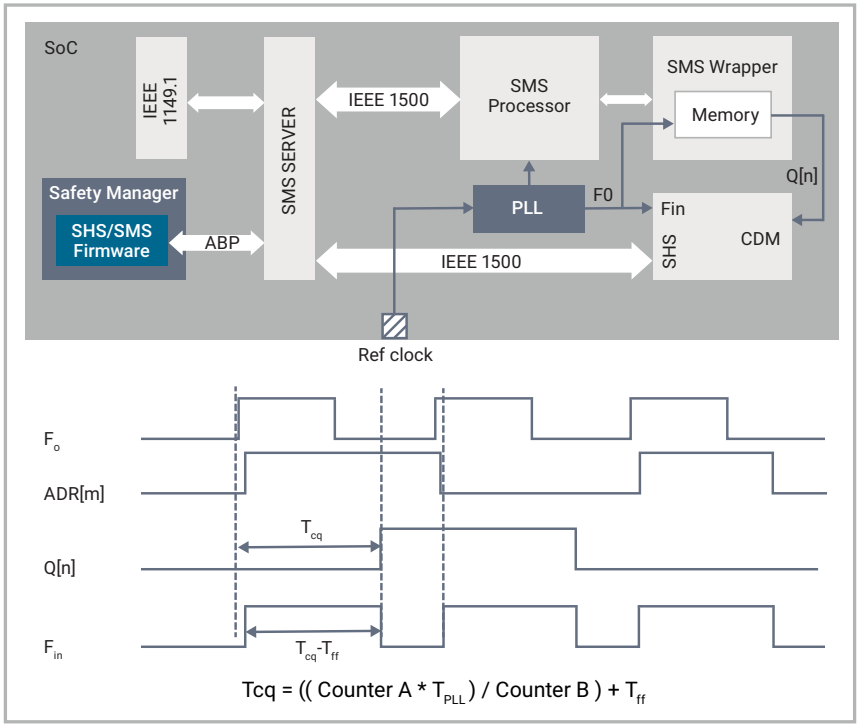

Figure 2: SHS/SMS based solution

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, PVT sensors, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors, and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits, and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.