DC Ultra

Concurrent Timing, Area, Power and Test Optimization

DC Ultra™ RTL synthesis solution enables users to meet today's design challenges with concurrent optimization of timing, area, power and test

Overview

DC Ultra includes innovative topographical technology that enables a predictable flow resulting in faster time to results.Topographical technology provides timing and area prediction within 10% of the results seen post-layout enabling designers to reduce costly iterations between synthesis and physical implementation. DC Ultra also includes a scalable infrastructure that delivers 2X faster runtime on quad-core platforms.

Key Benefits

- Concurrent optimization of timing, area, power and test
- Results correlate within 10% of physical implementation
- Removes timing bottlenecks by creating fast critical paths
- Gate-to-gate optimization for smaller area on new or legacy designs while maintaining timing Quality of Results (QoR)
- Cross-probing between RTL, schematic, and timing reports for fast debug
- Offers more flexibility for users to control optimization on specific areas of designs
- Enables higher efficiency with integrated static timing analysis, test synthesis and power synthesis
- Support for multi voltage and multi supply
- 2X faster runtime on quad-core compute servers

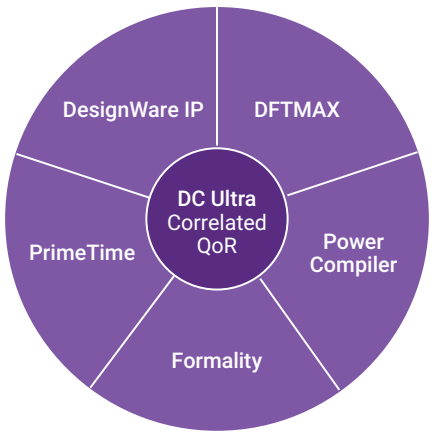

Figure 1: The industry's most comprehensive synthesis solution

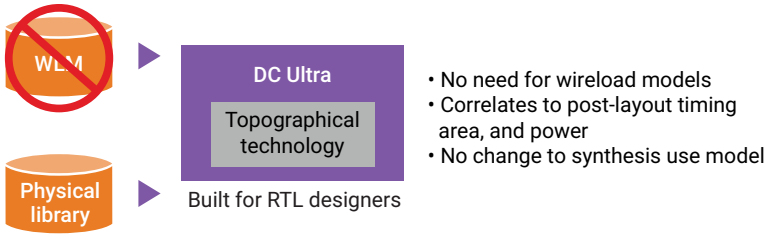

Figure 2: Topographical technology in RTL synthesis

Topographical Technology

Topographical technology delivers tight correlation to post-layout timing, area, test and power without the need for wireload models. It is designed for RTL designers and requires no physical design expertise or changes to the synthesis use model (Figure 2). Prediction of layout timing and area in DC Ultra is achieved through the innovative topographical technology.It enables RTL designers to fix real design issues while still in synthesis and generate a better starting point for place and route, eliminating costly iterations. This significantly boosts RTL designers' productivity. Topographical technology shares technology with Galaxy™ implementation, minimizing iterations to speed up physical implementation.

Area Reduction Technologies

DC Ultra provides optimization technologies that monotonically reduce gate-to-gate area by an average of 10% while maintaining Quality of Results (QoR). These advanced optimizations operate on both new and legacy design netlists, with or without physical information and at all process nodes. Area reductions are achieved without re-synthesis and without affecting timing results for maximum productivity.

Cross-Probing

Cross-probing between the RTL source code and other design views such as schematic, timing reports and physical implementation provide designers with the ability to quickly detect potential design issues and fix them at the source. Early visibility into potential design issues using multiple views accelerates the creation of high quality RTL and constraints.

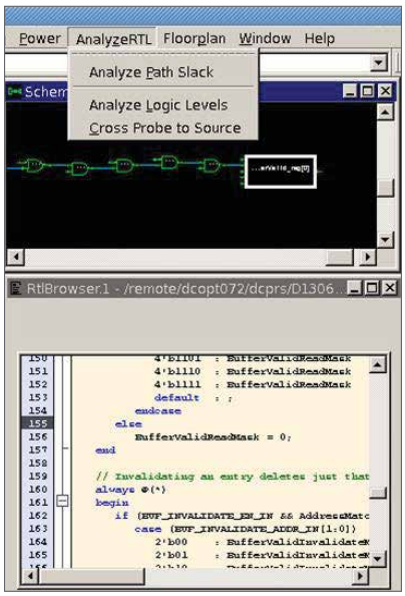

Figure 3: Cross-probing between RTL, schematic and timing view

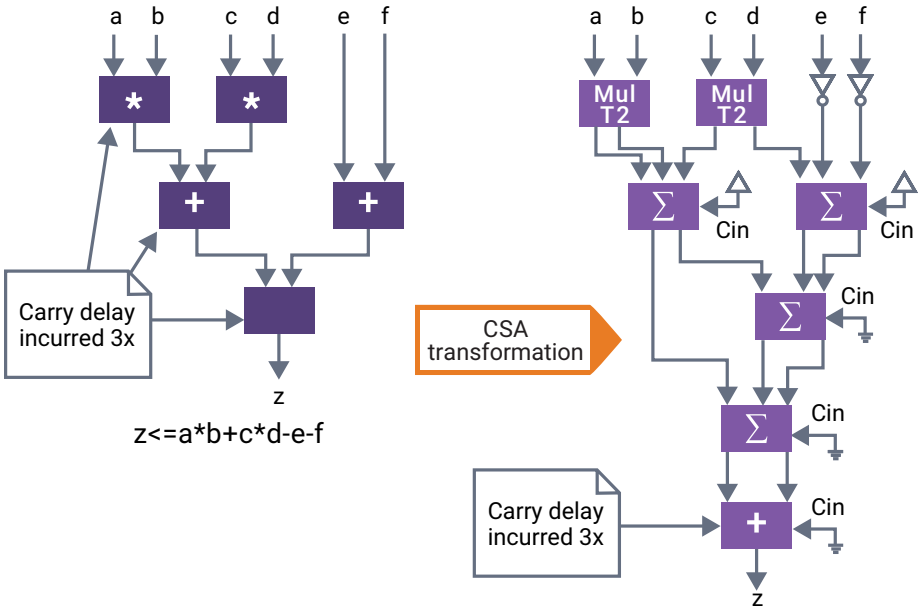

Figure 4: Transformation of sum of products into a Carry Save Adder (CSA) tree

Advanced Arithmetic Optimization

For designs containing datapath, DC Ultra uses innovative datapath optimization algorithms to achieve better quality-of results in terms of timing, area and power with fast runtimes. DC Ultra identifies arithmetic trees in your HDL and optimizes them using carrysave arithmetic techniques to minimize performance and area impact of carry propagation (Figure 4). With DC Ultra, logic synthesis users can also take advantage of superior datapath synthesis capability to generate highly optimized implementations of DesignWare arithmetic components.

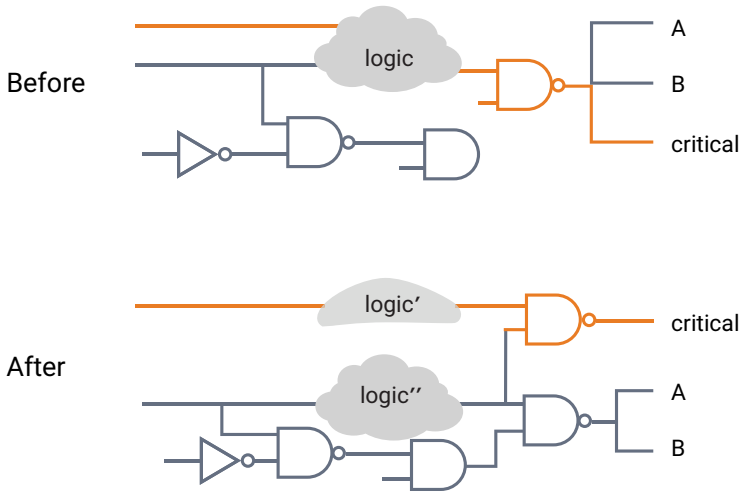

Figure 5: Through logic duplication, DC Ultra reduces the load on the critical path for significant timing improvements

Powerful Critical Path Synthesis

DC Ultra employs various optimization algorithms throughout the synthesis process to deliver ultra-fast critical path timing. For example, immediately after the initial technology mapping, the design is not yet subjected to detailed gate-level optimization techniques. At this stage, DC Ultra performs aggressive timing driven restructuring, mapping and gate-level optimization. As a result, the subsequent detailed gate-level optimizations benefit from better overall timing-based structure. Throughout gate-level optimization, additional strategies are applied to improve the delay of the critical paths in the design. One of the techniques includes aggressive logic duplication for reducing the load seen by the critical path (Figure 5). DC Ultra looks at a larger subsection of the critical path during logic duplication and can replicate many gates to reduce load of high fan-out nets, hence improving timing on critical paths through load isolation. DC Ultra will also automatically ungroup parts of the design on the critical path to achieve better area and timing. It can also buffer high fan-out nets to improve total negative slack.

The DC Ultra mapping algorithms also attempt to map groups of cells to wide fan-in library cells on critical timing paths that can reduce number of logic levels and cell instances. Thus, timing, area, and power are improved.

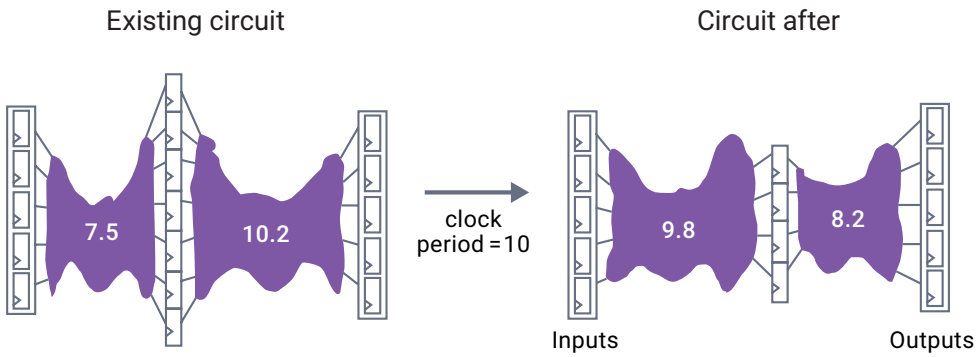

Figure 6: Retiming designs with registers

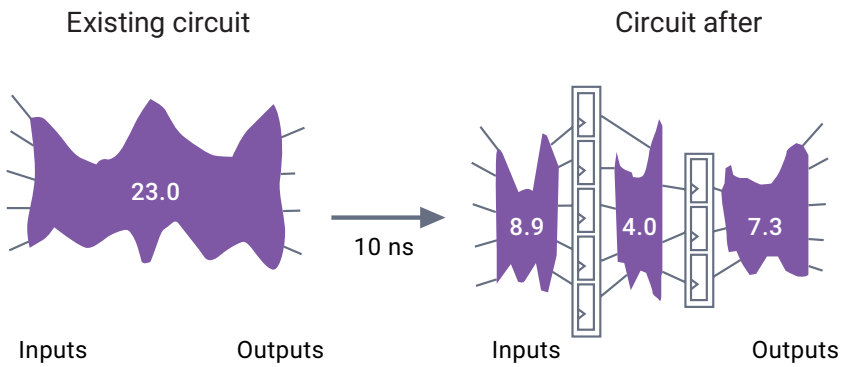

Figure 7: Retiming on combinational logic

Register Retiming

Register retiming further improves QoR. It performs optimization of sequential logic by moving registers through logic boundaries to optimize timing with minimum area impact (Figure 6) for designs that already contain registers. The same functionality is preserved at I/O boundaries. Register retiming can also insert pipeline registers in pure combination circuits to be used to meet performance requirements as well as reduce area (Figure 7). Register retiming can be used along with datapath optimization algorithms to get the fastest pipelines.

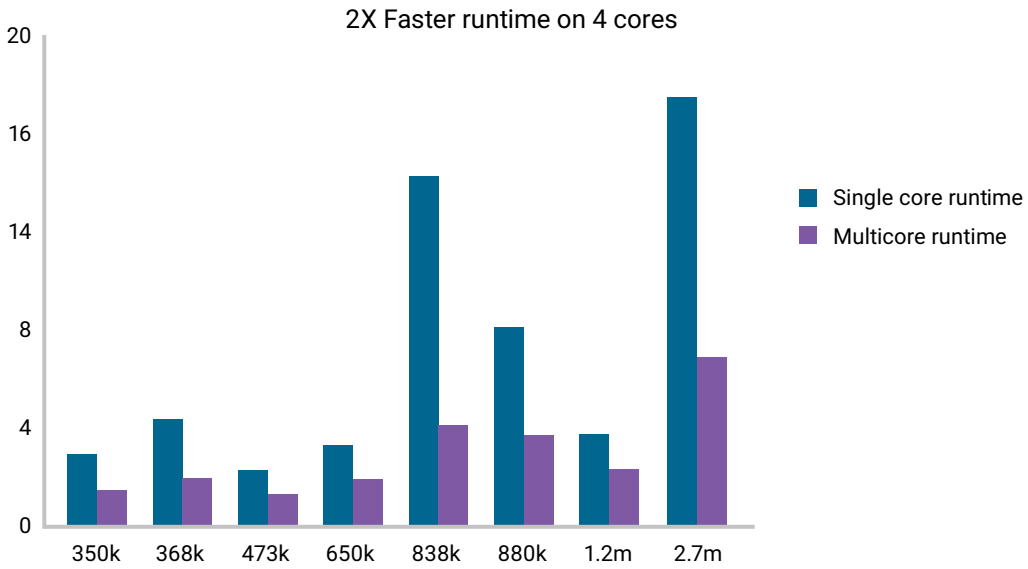

Figure 8: Synthesis runtime

Better Control of Synthesis Cost-Function Priorities and Optimization Steps

DC Ultra provides finer control over optimization to meet aggressive timing requirements. DC Ultra has a default cost function that prioritizes design rule requirements over timing and area constraints. By setting the appropriate priority, designers can drive synthesis to achieve the best QoR for a design. Compile directives in DC Ultra can be used to further control optimization. The compile directives allow the designer to change DC Ultra's standard behavior. For example, a designer may have a particular structure in mind and have instantiated the cells in the path. Although the overall structure should not change, it may be desirable for Design Compiler to perform sizing and local optimization for better timing. For this set of optimizations, the global structuring of the logic can be disabled while enabling gate sizing.

Infrastructure for Multicore

The advent of multicore processors in computer platforms has boosted the processing power available to designers. DC Ultra includes a scalable infrastructure to take advantage of multicore compute servers. Using an optimized scheme of distributed and multithreaded parallelization, DC Ultra delivers a 2X improvement in runtimes on quad core platforms. The infrastructure delivers runtime benefits without deviating from the quality of results. Figure 8 compares DC Ultra runtimes across multiple designs on single core vs. quad core machines. On the X-axis are designs and on the Y-axis are the runtimes in hours. The blue bars represent DC Ultra runtimes using a single core machine and the purple bars represent runtimes using quad core machines for the same design. As seen in the figure, DC Ultra is, on average, 2X faster on quad core compute servers.

Netlist Formats and Interfaces

DC Ultra supports all popular industry standard formats:

Circuit Netlist:

- Verilog, SystemVerilog, and VHDL
- Command Script: dcsh, TCL

Interfaces:

- PLI, SDF, PDEF, SDC

Platforms:

- IBM AIX (32-/64-bit)
- Redhat Linux (32-/64-bit)
- Sun Solaris (32-/64-bit)

Summary

DC Ultra includes comprehensive algorithms to optimize concurrently for timing, area, power and test. The topographical technology in DC Ultra ensures that results correlate to layout, eliminating costly iterations between synthesis and physical implementation. Optimization technologies that reduce gate-to-gate area by an average of 10% while maintaining timing Quality of Results (QoR) operate on both new and legacy design netlists. RTL cross-probing with multiple design views accelerates creation of high quality RTL and constraints.

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